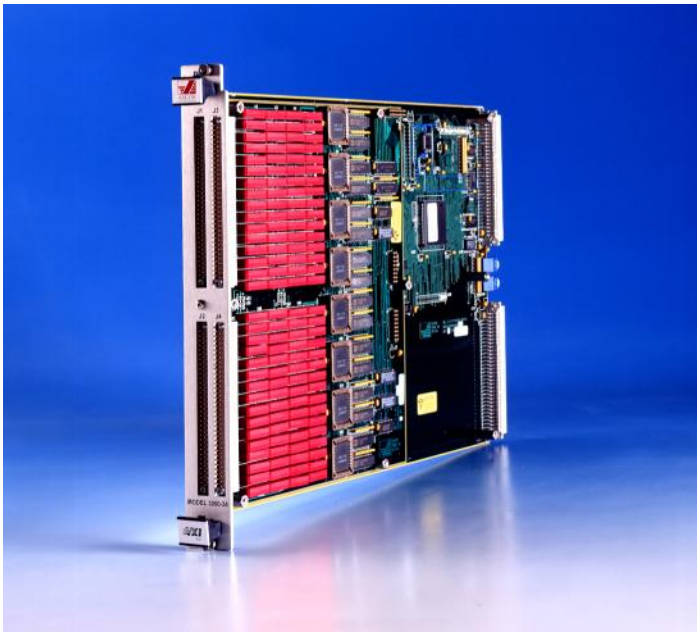
Model 3000-34
4(2x32) Matrix
90400190



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CONTACT INFORMATION

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Regulatory compliance information

This product complies with the essential requirements of the following applicable European Directives, and carries the CE mark accordingly.

89/336/EEC and 73/23/EEC	EMC Directive and Low Voltage Directive
EN61010-1 (1993)	Electrical Safety
EN61326-1 (1997)	EMC – Emissions and Immunity
Manufacturer's Name:	**Manufacturer's Address**
Giga-tronics, Incorporated	4650 Norris Canyon Road San Ramon, California 94583 U.S.A.
Type of Equipment:	**Model Series Number**
Switching Module	3000-34

Declaration of Conformity on file. Contact Giga-tronics at the following;

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Record of Changes to This Manual

Use the table below to maintain a permanent record of changes to this document. Corrected replacement pages are issued as Technical Publication Change Instructions (TPCI). When you are issued a TPCI, do the following:

1. Insert the TPCI at the front of the manual binder.
2. Remove the pages from the manual binder that are noted in the TPCI.
3. Replace the page(s) removed in the previous step with the corrected page(s).
4. Record the changes in the table below.

TPCI Number	TPCI Issue Date	Date Entered	Comments

Revision History			
Revision	**Description of Change**	**Chg Order #**	**Approved By**
A	Initial Release		
B	Updated		
C	Reformatted 2/12		RCW

Contents

Chapter 1 **Introduction**

1.1 Safety and Manual Conventions

This manual contains conventions regarding safety and equipment usage as described below.

1.1.1 Product Reference

Throughout this manual, the term “Common Core Switching Platform, Series 8800” refers to all models of within the series, unless otherwise specified.

1.1.2 Personal Safety Alert

WARNING: Indicates a hazardous situation which, if not avoided, could result in death or serious injury.

1.1.3 Equipment Safety Alert

CAUTION **CAUTION:** Indicates a situation which can damage or adversely affect the product or associated equipment.

1.1.4 Notes

Notes are denoted and used as follows:

NOTE: Highlights or amplifies an essential operating or maintenance procedure, practice, condition or statement.

1.1.5 Electrical Safety Precautions

Any servicing instructions are for use by service-trained personnel only. To avoid personal injury, do not perform any service unless you are qualified to do so.

For continued protections against fire hazard, replace the AC line fuse only with a fuse of the same current rating and type. Do not use repaired fuses or short circuited fuse holders.

Chapter 2 **Configuration Table**

PL 90400190 SINGLE 2x128

ASSY 90400190

PL 85001810

ASSY 85001810

SCH 85001810

PL 85001820

ASSY 85001820

SCH 85001820

PL 90400190-001 QUAD 2x32

ASSY 90400190-001

PL 85001810-001

ASSY 85001810-001

SCH 85001810

PL 85001820-001

ASSY 85001820-001

SCH 85001820

Chapter 3 **Functional Description**

The Module 3000-34 is a VXI compatible unit. This module contains matrices which can be jumper-configured for 2x64 or dual 2x32 switch matrices. With an additional, optional daughterboard this module can be expanded to a single 2x128, dual 2x64 or quad 2x32 configuration.

Each relay can be individually controlled. Any and all relays can be closed. The switch matrices are specially designed to support Automatic Test Equipment (ATE), and they are designed to support shielded instruments.

This module is ideal for supporting general purpose switching, multi-channel stimulus or measurement switch matrices. Each switch is shielded to a common shield plane. This switch printed circuit board (PCB) is a multi-layer design with 50 ohm microstrip for optimum signal performance. The Interface and mechanical construction meets the specifications of the VXIbus System Specification, Rev 1.2 and Rev 1.3.

The Model 3000-34 provides high quality general purpose switching for selecting signals to be routed from a selected pin to any two channels. This module was designed with special shielding for high quality signal switching and low noise. This module is ideal for general purpose scanners and many other switching operations where multiple inputs can be routed to any two channels.

Each switch is coaxially shielded to an isolated ground plane which is designated as “shield.” The shield is connected through the front panel connectors. The module can be configured for one of the following matrix configurations:

One 2x64. Any signal can be routed from channels A or B to any of the 64 front panel connector pins. Up to two simultaneous channels can be programmed.

Dual 2x32. Any signal can be routed from channels A or B to any of 32 pins on the front panel connectors, and any signal can be routed from channels C or D to the other 32 pins. Up to two simultaneous channels can be programmed per matrix or four simultaneous channels.

Dual 2x64. Any signal can be routed from channels A or B to any of 64 front panel connector pins, and any signal can be routed from channels C and D to another 64 pins. Up to two simultaneous channels can be programmed per matrix or four simultaneous channels.

Quad 2x32. Any signal can be routed from channels A or B to any of 32 pins. Any signal can be routed from channels C or D to another 32 pins. Any signal can be routed from channels E or F to another 32 pins. Any signal can be routed from channels G or H to another 32 pins. Up to two simultaneous channels can be programmed per matrix or eight simultaneous channels.

Single 2x128. Any signal can be routed from channels A or B to any of 128 pins on the front panel connectors. Up to two simultaneous channels can be programmed.

Chapter 4 Theory of Operation

The main circuit board assembly contains the VXI interface and the basic 2x64 or dual 2x32 switch matrices. This can be jumper configured to the desired matrix. (See Daughterboard Jumper Configuration in Section 3 of this manual). A daughter circuit card assembly is added to provide an additional dual 2x32 or 2x64 set of relays. The total switch configuration then provides a single 2x128, dual 2x64 or quad 2x32.

The basic module is a register based VXI module. It is a register Dynamic Configuration (DC) device, wherein the Resource Manager software running on the slot-0 controller/computer determines the A16 and A24 address space. Refer to the VXI System Specifications.

A library cell is made SC (Static Configuration) by changing the address switches from FFh to a value in the range 01h-FEh. Each card in the VXI system must have its own A16 address.

The main circuit card assembly contains the basic switch matrices and VXI interface. There are 128 relays which are used to configure a dual 2x32 relay matrix or 2x64 matrix. Relay control is through eight 16-bit registers at A24 offsets 40h to 4Eh. U104-107 and U109-112 are the VXI interface circuits. U111 is a custom gate array which contains the VXI interface. It provides the A16, A24 and A32 bit addressing capability for the module. U104, U105, U106, U109 and U110 are buffers to the VXI plane. U112 is the interrupt interface buffer.

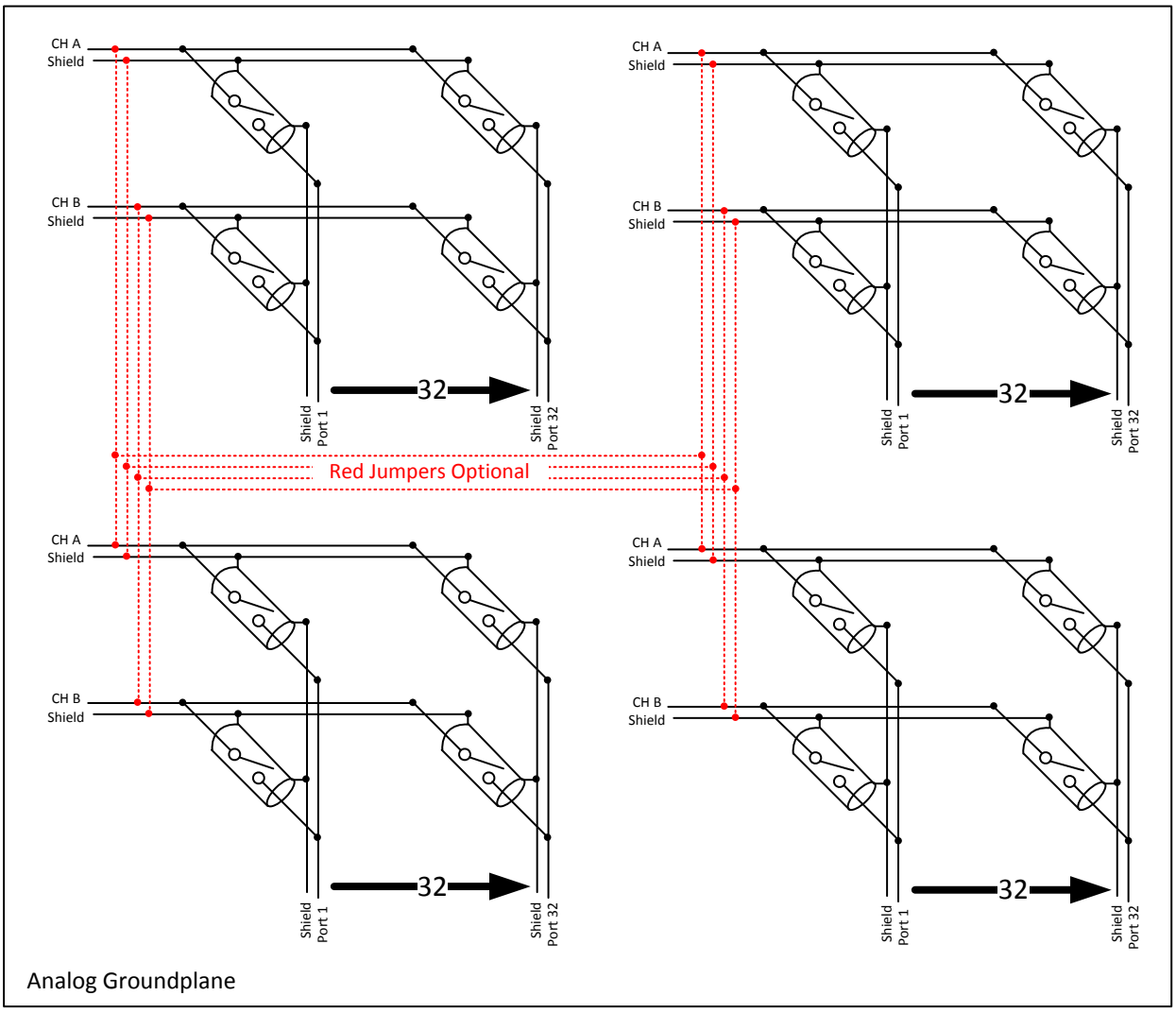
U7 and U8 are data buffers, and U32 and U33 are buffers to the additional Daughterboard. U13, U29 and U30 are the address decoders to gain access to the relay registers. The relay registers and drivers are combined into a 16-bit interface driver chip.

Each device contains a 16-bit readable register and 16 open collector relay drivers with suppression diodes. These are transceivers to monitor the relay drive level. The host controller can read the contents of the program register of the logic level of the relay coil. This allows self test of the circuit to isolate between register or coil errors.

The registers are U1, U4, U9, U14, U17, U20, U23 and U26. The coil read-back is provided by U2, U3, U5, U6, U10, U11, U15, U16, U18, U19, U21, U22, U24, U25, U27 and U28. In the schematic, a map of the pin assignments is given.

The daughterboard is a duplicate of the switch matrices on the main circuit. It provides an additional dual 2x32 or 2x64 expansion switch matrices. This daughterboard plugs on top of the Motherboard and interfaces to U32, U33. U7, U8, U12, U13, U30, U31, U39 are the interface to the Motherboard. These are the data buffer, address decoders to the relay register/drivers. The organization and names of the relay drivers are the same as on the Motherboard described above. The registers are U1, U4, U9, U14, U17, U20, U23 and U26. U2, U3, U5, U6, U10, U11, U15, U16, U18, U19, U21, U22, U24, U25, U27 and U28 are the transceivers for reading the coil state.

Chapter 5 **Block Diagram**



Chapter 6 Controls and Indicators

The following controls and indicators are provided to select and display the functions of the ASCOR 3000-34 Module's operating environment.

6.1 VXI LOGICAL ADDRESS

See the Logical Address Switch setting in the Installation and Maintenance section

located in Section 2 .

6.2 LEDs

The following LEDs are visible at the Module's front panel to indicate the

status of the module's operation:

6.2.1 "BUS" LED

This green color LED is normally off and will flash on when the 3000-34

module is addressed by the system.

6.2.2 "PWR" LED

This red color LED is normally on when the board is in operation.

Chapter 7 Internal Settings

The following items are inside the module and can be reached by removing the side cover.

7.1 FUSE

The ASCOR VXI 3000-34 uses a 10 Amp fuse in the +5 Volt line and is located on

the Mother Board (MB) assembly.

7.2 VXI_{bus} INTERRUPT LEVEL SELECTION

The VXIbus interrupt level is set with three bits in the "3Eh" register.

See the section on "A16 ADDRESS SPACE REGISTER DESCRIPTION".

The interrupt level is factory set to "no interrupt".

Chapter 8 **Specifications**

Single slot VXI “C” size module

Programming is register based *VXIPlug&play*

VXI power	+5 volts @ 1.5 A
Max. Switching Voltage (DC, peak resistive)	200 Volts
Max. Switching Current (DC, peak resistive)	0.5 Amp
Max Carry Current (DC, peak resistive)	1.0 Amp
Max Switching Power	10 Watts
Life Expectancy w/signal <1.0V, 0.01 Amp	5,000,000 cycles
Contact Resistance	0.30 ohms
Isolation	100,000,000 ohms
Bandwidth:	
2x128	12 MHz
2x64	24 MHz
2x32	55 MHz
Crosstalk channel to channel	>-30 dB

Chapter 10 **Register Map**

Register 40h (Motherboard)
Function: Control Matrix pins 1-8.

BIT	FUNCTION	COMMENTS
0	Chan A, Pin 1	J1-33, Shield: J1-66
1	Chan A, Pin 2	J1-32, Shield: J1-65
2	Chan A, Pin 3	J1-31, Shield: J1-64
3	Chan A, Pin 4	J1-30, Shield: J1-63
4	Chan A, Pin 5	J1-29, Shield: J1-62
5	Chan A, Pin 6	J1-28, Shield: J1-61
6	Chan A, Pin 7	J1-27, Shield: J1-60
7	Chan A, Pin 8	J1-26, Shield: J1-59
8	Chan B, Pin 1	J1-33, Shield: J1-66
9	Chan B, Pin 2	J1-32, Shield: J1-65
10	Chan B, Pin 3	J1-31, Shield: J1-64
11	Chan B, Pin 4	J1-30, Shield: J1-63
12	Chan B, Pin 5	J1-29, Shield: J1-62
13	Chan B, Pin 6	J1-28, Shield: J1-61
14	Chan B, Pin 7	J1-27, Shield: J1-60
15	Chan B, Pin 8	J1-26, Shield: J1-59

note: Channel A is on J1-37, shield is on J1-36
Channel B is on J1-35, shield is on J1-34

Register 42h (Motherboard)
Function: Control Matrix pins 9-16.

BIT	FUNCTION	COMMENTS
0	Chan A, Pin 9	J1-25, Shield: J1-58
1	Chan A, Pin 10	J1-24, Shield: J1-57
2	Chan A, Pin 11	J1-23, Shield: J1-56
3	Chan A, Pin 12	J1-22, Shield: J1-55
4	Chan A, Pin 13	J1-21, Shield: J1-54
5	Chan A, Pin 14	J1-20, Shield: J1-53
6	Chan A, Pin 15	J1-19, Shield: J1-52
7	Chan A, Pin 16	J1-18, Shield: J1-51
8	Chan B, Pin 9	J1-25, Shield: J1-58
9	Chan B, Pin 10	J1-24, Shield: J1-57
10	Chan B, Pin 11	J1-23, Shield: J1-56
11	Chan B, Pin 12	J1-22, Shield: J1-55
12	Chan B, Pin 13	J1-21, Shield: J1-54
13	Chan B, Pin 14	J1-20, Shield: J1-53
14	Chan B, Pin 15	J1-19, Shield: J1-52
15	Chan B, Pin 16	J1-18, Shield: J1-51

note: Channel A is on J1-37, shield is on J1-36
Channel B is on J1-35, shield is on J1-34

Register 44h (Motherboard)
Function: Control Matrix pins 17-24.

BIT	FUNCTION	COMMENTS
0	Chan A, Pin 17	J1-17, Shield: J1-50
1	Chan A, Pin 18	J1-16, Shield: J1-49
2	Chan A, Pin 19	J1-15, Shield: J1-48
3	Chan A, Pin 20	J1-14, Shield: J1-47
4	Chan A, Pin 21	J1-13, Shield: J1-46
5	Chan A, Pin 22	J1-12, Shield: J1-45
6	Chan A, Pin 23	J1-11, Shield: J1-44
7	Chan A, Pin 24	J1-10, Shield: J1-43
8	Chan B, Pin 17	J1-17, Shield: J1-50
9	Chan B, Pin 18	J1-16, Shield: J1-49
10	Chan B, Pin 19	J1-15, Shield: J1-48
11	Chan B, Pin 20	J1-14, Shield: J1-47
12	Chan B, Pin 21	J1-13, Shield: J1-46
13	Chan B, Pin 22	J1-12, Shield: J1-45
14	Chan B, Pin 23	J1-11, Shield: J1-44
15	Chan B, Pin 24	J1-10, Shield: J1-43

note: Channel A is on J1-37, shield is on J1-36
Channel B is on J1-35, shield is on J1-34

Register 46h (Motherboard)
Function: Control Matrix pins 25-32.

BIT	FUNCTION	COMMENTS
0	Chan A, Pin 25	J1- 9, Shield: J1-42
1	Chan A, Pin 26	J1- 8, Shield: J1-41
2	Chan A, Pin 27	J1- 7, Shield: J1-40
3	Chan A, Pin 28	J1- 6, Shield: J1-39
4	Chan A, Pin 29	J1- 5, Shield: J1-38
5	Chan A, Pin 30	J1- 4, Shield: J1-36
6	Chan A, Pin 31	J1- 3, Shield: J1-36
7	Chan A, Pin 32	J1- 2, Shield: J1-34
8	Chan B, Pin 25	J1- 9, Shield: J1-42
9	Chan B, Pin 26	J1- 8, Shield: J1-41
10	Chan B, Pin 27	J1- 7, Shield: J1-40
11	Chan B, Pin 28	J1- 6, Shield: J1-39
12	Chan B, Pin 29	J1- 5, Shield: J1-38
13	Chan B, Pin 30	J1- 4, Shield: J1-36
14	Chan B, Pin 31	J1- 3, Shield: J1-36
15	Chan B, Pin 32	J1- 2, Shield: J1-34

note: Channel A is on J1-37, shield is on J1-36
Channel B is on J1-35, shield is on J1-34
Chassis ground is on J1-1

Register 48h (Motherboard)

Function: Control Matrix pins: 1-8 (channel C, D) for dual 2 X 32
1-8 (channel C, D) for quad 2 X 32
1-8 (channel C, D) for dual 2 X 64
33-40 (channel A, B) for 2 X 64
33-40 (channel A, B) for 2 X 128

BIT	FUNCTION	COMMENTS
0	Chan C, Pin 1	J2-33, Shield: J2-66
1	Chan C, Pin 2	J2-32, Shield: J2-65
2	Chan C, Pin 3	J2-31, Shield: J2-64
3	Chan C, Pin 4	J2-30, Shield: J2-63
4	Chan C, Pin 5	J2-29, Shield: J2-62
5	Chan C, Pin 6	J2-28, Shield: J2-61
6	Chan C, Pin 7	J2-27, Shield: J2-60
7	Chan C, Pin 8	J2-26, Shield: J2-59
8	Chan D, Pin 1	J2-33, Shield: J2-66
9	Chan D, Pin 2	J2-32, Shield: J2-65
10	Chan D, Pin 3	J2-31, Shield: J2-64
11	Chan D, Pin 4	J2-30, Shield: J2-63
12	Chan D, Pin 5	J2-29, Shield: J2-62
13	Chan D, Pin 6	J2-28, Shield: J2-61
14	Chan D, Pin 7	J2-27, Shield: J2-60
15	Chan D, Pin 8	J2-26, Shield: J2-59

note: Channel C is on J2-37, shield is on J2-36
Channel D is on J2-35, shield is on J2-34

Register 4Ah (Motherboard)

Function: Control Matrix pins:

9-16 (channel C, D) for dual 2 X 32
9-16 (channel C, D) for quad 2 X 32
9-16 (channel C, D) for dual 2 X 64
41-48 (channel A, B) for 2 X 64
41-48 (channel A, B) for 2 X 128

BIT	FUNCTION	COMMENTS
0	Chan C, Pin 9	J2-25, Shield: J2-58
1	Chan C, Pin 10	J2-24, Shield: J2-57
2	Chan C, Pin 11	J2-23, Shield: J2-56
3	Chan C, Pin 12	J2-22, Shield: J2-55
4	Chan C, Pin 13	J2-21, Shield: J2-54
5	Chan C, Pin 14	J2-20, Shield: J2-53
6	Chan C, Pin 15	J2-19, Shield: J2-52
7	Chan C, Pin 16	J2-18, Shield: J2-51
8	Chan D, Pin 9	J2-25, Shield: J2-58
9	Chan D, Pin 10	J2-24, Shield: J2-57
10	Chan D, Pin 11	J2-23, Shield: J2-56
11	Chan D, Pin 12	J2-22, Shield: J2-55
12	Chan D, Pin 13	J2-21, Shield: J2-54
13	Chan D, Pin 14	J2-20, Shield: J2-53
14	Chan D, Pin 15	J2-19, Shield: J2-52
15	Chan D, Pin 16	J2-18, Shield: J2-51

note: Channel C is on J2-37, shield is on J2-36
Channel D is on J2-35, shield is on J2-34

Register 4Ch (Motherboard)

Function: Control Matrix pins: 17-24 (channel C, D) for dual 2 X 32
17-24 (channel C, D) for quad 2 X 32
17-24 (channel C, D) for dual 2 X 64
49-56 (channel A, B) for 2 X 64
49-56 (channel A, B) for 2 X 128

BIT	FUNCTION	COMMENTS
0	Chan C, Pin 17	J2-17, Shield: J2-50
1	Chan C, Pin 18	J2-16, Shield: J2-49
2	Chan C, Pin 19	J2-15, Shield: J2-48
3	Chan C, Pin 20	J2-14, Shield: J2-47
4	Chan C, Pin 21	J2-13, Shield: J2-46
5	Chan C, Pin 22	J2-12, Shield: J2-45
6	Chan C, Pin 23	J2-11, Shield: J2-44
7	Chan C, Pin 24	J2-10, Shield: J2-43
8	Chan D, Pin 17	J2-17, Shield: J2-50
9	Chan D, Pin 18	J2-16, Shield: J2-49
10	Chan D, Pin 19	J2-15, Shield: J2-48
11	Chan D, Pin 20	J2-14, Shield: J2-47
12	Chan D, Pin 21	J2-13, Shield: J2-46
13	Chan D, Pin 22	J2-12, Shield: J2-45
14	Chan D, Pin 23	J2-11, Shield: J2-44
15	Chan D, Pin 24	J2-10, Shield: J2-43

note: Channel C is on J2-37, shield is on J2-36
Channel D is on J2-35, shield is on J2-34

Register 4Eh (Motherboard)

Function: Control Matrix pins:

25-32 (channel C, D) for dual 2 X 32
25-32 (channel C, D) for quad 2 X 32
25-32 (channel C, D) for dual 2 X 64
57-64 (channel A, B) for 2 X 64
57-64 (channel A, B) for 2 X 128

BIT	FUNCTION	COMMENTS
0	Chan C, Pin 25	J2- 9, Shield: J2-42
1	Chan C, Pin 26	J2- 8, Shield: J2-41
2	Chan C, Pin 27	J2- 7, Shield: J2-40
3	Chan C, Pin 28	J2- 6, Shield: J2-39
4	Chan C, Pin 29	J2- 5, Shield: J2-38
5	Chan C, Pin 30	J2- 4, Shield: J2-36
6	Chan C, Pin 31	J2- 3, Shield: J2-36
7	Chan C, Pin 32	J2- 2, Shield: J2-34
8	Chan D, Pin 25	J2- 9, Shield: J2-42
9	Chan D, Pin 26	J2- 8, Shield: J2-41
10	Chan D, Pin 27	J2- 7, Shield: J2-40
11	Chan D, Pin 28	J2- 6, Shield: J2-39
12	Chan D, Pin 29	J2- 5, Shield: J2-38
13	Chan D, Pin 30	J2- 4, Shield: J2-36
14	Chan D, Pin 31	J2- 3, Shield: J2-36
15	Chan D, Pin 32	J2- 2, Shield: J2-34

note: Channel C is on J2-37, shield is on J2-36
Channel D is on J2-35, shield is on J2-34
Chassis ground is on J2-1

Register Map
Model 3000-34
Daughterboard
Register 50h (Daughterboard)
Function: Control Matrix pins : 1-8 (channel E, F) for quad 2 X 32
33-40 (channel A, B) for dual 2 X 64
65-72 (channel A, B) for 2 X 128

BIT	FUNCTION	COMMENTS
0	Chan E, Pin 1	J3-33, Shield: J3-66
1	Chan E, Pin 2	J3-32, Shield: J3-65
2	Chan E, Pin 3	J3-31, Shield: J3-64
3	Chan E, Pin 4	J3-30, Shield: J3-63
4	Chan E, Pin 5	J3-29, Shield: J3-62
5	Chan E, Pin 6	J3-28, Shield: J3-61
6	Chan E, Pin 7	J3-27, Shield: J3-60
7	Chan E, Pin 8	J3-26, Shield: J3-59
8	Chan F, Pin 1	J3-33, Shield: J3-66
9	Chan F, Pin 2	J3-32, Shield: J3-65
10	Chan F, Pin 3	J3-31, Shield: J3-64
11	Chan F, Pin 4	J3-30, Shield: J3-63
12	Chan F, Pin 5	J3-29, Shield: J3-62
13	Chan F, Pin 6	J3-28, Shield: J3-61
14	Chan F, Pin 7	J3-27, Shield: J3-60
15	Chan F, Pin 8	J3-26, Shield: J3-59

note: Channel E is on J3-37, shield is on J3-36
Channel F is on J3-35, shield is on J3-34

Register 52h (Daughterboard)
Function: Control Matrix pins: 9-16 (channel E, F) for quad 2 X 32
41-48 (channel A, B) for dual 2 X 64
73-80 (channel A, B) for 2 X 128

BIT	FUNCTION	COMMENTS
0	Chan E, Pin 9	J3-25, Shield: J3-58
1	Chan E, Pin 10	J3-24, Shield: J3-57
2	Chan E, Pin 11	J3-23, Shield: J3-56
3	Chan E, Pin 12	J3-22, Shield: J3-55
4	Chan E, Pin 13	J3-21, Shield: J3-54
5	Chan E, Pin 14	J3-20, Shield: J3-53
6	Chan E, Pin 15	J3-19, Shield: J3-52
7	Chan E, Pin 16	J3-18, Shield: J3-51
8	Chan F, Pin 9	J3-25, Shield: J3-58
9	Chan F, Pin 10	J3-24, Shield: J3-57
10	Chan F, Pin 11	J3-23, Shield: J3-56
11	Chan F, Pin 12	J3-22, Shield: J3-55
12	Chan F, Pin 13	J3-21, Shield: J3-54
13	Chan F, Pin 14	J3-20, Shield: J3-53
14	Chan F, Pin 15	J3-19, Shield: J3-52
15	Chan F, Pin 16	J3-18, Shield: J3-51

note: Channel E is on J3-37, shield is on J3-36
Channel F is on J3-35, shield is on J3-34

Register 54h (Daughterboard)
Function: Control Matrix pins: 17-24 (channel E, F) for quad 2 X 32
49-56 (channel A, B) for dual 2 X 64
81-88 (channel A, B) for 2 X 128

BIT	FUNCTION	COMMENTS
0	Chan E, Pin 17	J3-17, Shield: J3-50
1	Chan E, Pin 18	J3-16, Shield: J3-49
2	Chan E, Pin 19	J3-15, Shield: J3-48
3	Chan E, Pin 20	J3-14, Shield: J3-47
4	Chan E, Pin 21	J3-13, Shield: J3-46
5	Chan E, Pin 22	J3-12, Shield: J3-45
6	Chan E, Pin 23	J3-11, Shield: J3-44
7	Chan E, Pin 24	J3-10, Shield: J3-43
8	Chan F, Pin 17	J3-17, Shield: J3-50
9	Chan F, Pin 18	J3-16, Shield: J3-49
10	Chan F, Pin 19	J3-15, Shield: J3-48
11	Chan F, Pin 20	J3-14, Shield: J3-47
12	Chan F, Pin 21	J3-13, Shield: J3-46
13	Chan F, Pin 22	J3-12, Shield: J3-45
14	Chan F, Pin 23	J3-11, Shield: J3-44
15	Chan F, Pin 24	J3-10, Shield: J3-43

note: Channel E is on J3-37, shield is on J3-36
Channel F is on J3-35, shield is on J3-34

Register 56h (Daughterboard)
Function: Control Matrix pins: 25-32 (channel E, F) for quad 2 X 32
57-64 (channel A, B) for dual 2 X 64
89-96 (channel A, B) for 2 X 128

BIT	FUNCTION	COMMENTS
0	Chan E, Pin 25	J3- 9, Shield: J3-42
1	Chan E, Pin 26	J3- 8, Shield: J3-41
2	Chan E, Pin 27	J3- 7, Shield: J3-40
3	Chan E, Pin 28	J3- 6, Shield: J3-39
4	Chan E, Pin 29	J3- 5, Shield: J3-38
5	Chan E, Pin 30	J3- 4, Shield: J3-36
6	Chan E, Pin 31	J3- 3, Shield: J3-36
7	Chan E, Pin 32	J3- 2, Shield: J3-34
8	Chan F, Pin 25	J3- 9, Shield: J3-42
9	Chan F, Pin 26	J3- 8, Shield: J3-41
10	Chan F, Pin 27	J3- 7, Shield: J3-40
11	Chan F, Pin 28	J3- 6, Shield: J3-39
12	Chan F, Pin 29	J3- 5, Shield: J3-38
13	Chan F, Pin 30	J3- 4, Shield: J3-36
14	Chan F, Pin 31	J3- 3, Shield: J3-36
15	Chan F, Pin 32	J3- 2, Shield: J3-34

note: Channel E is on J3-37, shield is on J3-36
Channel F is on J3-35, shield is on J3-34
Chassis ground is on J3-1

Register 58h (Daughterboard)
Function: Control Matrix pins: 1-8 (channel G, H) for quad 2 X 32
33-40 (channel C, D) for dual 2 X 64
97-104 (channel A, B) for 2 X 128

BIT	FUNCTION	COMMENTS
0	Chan G, Pin 1	J4-33, Shield: J4-66
1	Chan G, Pin 2	J4-32, Shield: J4-65
2	Chan G, Pin 3	J4-31, Shield: J4-64
3	Chan G, Pin 4	J4-30, Shield: J4-63
4	Chan G, Pin 5	J4-29, Shield: J4-62
5	Chan G, Pin 6	J4-28, Shield: J4-61
6	Chan G, Pin 7	J4-27, Shield: J4-60
7	Chan G, Pin 8	J4-26, Shield: J4-59
8	Chan H, Pin 1	J4-33, Shield: J4-66
9	Chan H, Pin 2	J4-32, Shield: J4-65
10	Chan H, Pin 3	J4-31, Shield: J4-64
11	Chan H, Pin 4	J4-30, Shield: J4-63
12	Chan H, Pin 5	J4-29, Shield: J4-62
13	Chan H, Pin 6	J4-28, Shield: J4-61
14	Chan H, Pin 7	J4-27, Shield: J4-60
15	Chan H, Pin 8	J4-26, Shield: J4-59

note: Channel G is on J4-37, shield is on J4-36
Channel H is on J4-35, shield is on J4-34

Register 5Ah (Daughterboard)
Function: Control Matrix pins: 9-16 (channel G, H) for quad 2 X 32
41-48 (channel C, D) for dual 2 X 64
105-112 (channel A, B) for 2 X 128

BIT	FUNCTION	COMMENTS
0	Chan G, Pin 9	J4-25, Shield: J4-58
1	Chan G, Pin 10	J4-24, Shield: J4-57
2	Chan G, Pin 11	J4-23, Shield: J4-56
3	Chan G, Pin 12	J4-22, Shield: J4-55
4	Chan G, Pin 13	J4-21, Shield: J4-54
5	Chan G, Pin 14	J4-20, Shield: J4-53
6	Chan G, Pin 15	J4-19, Shield: J4-52
7	Chan G, Pin 16	J4-18, Shield: J4-51
8	Chan H, Pin 9	J4-25, Shield: J4-58
9	Chan H, Pin 10	J4-24, Shield: J4-57
10	Chan H, Pin 11	J4-23, Shield: J4-56
11	Chan H, Pin 12	J4-22, Shield: J4-55
12	Chan H, Pin 13	J4-21, Shield: J4-54
13	Chan H, Pin 14	J4-20, Shield: J4-53
14	Chan H, Pin 15	J4-19, Shield: J4-52
15	Chan H, Pin 16	J4-18, Shield: J4-51

note: Channel G is on J4-37, shield is on J4-36
Channel H is on J4-35, shield is on J4-34

Register 5Ch (Daughterboard)
Function: Control Matrix pins: 17-24 (channel G, H) for quad 2 X 32
49-56 (channel C, D) for dual 2 X 64
113-120 (channel A, B) for 2 X 128

BIT	FUNCTION	COMMENTS
0	Chan G, Pin 17	J4-17, Shield: J4-50
1	Chan G, Pin 18	J4-16, Shield: J4-49
2	Chan G, Pin 19	J4-15, Shield: J4-48
3	Chan G, Pin 20	J4-14, Shield: J4-47
4	Chan G, Pin 21	J4-13, Shield: J4-46
5	Chan G, Pin 22	J4-12, Shield: J4-45
6	Chan G, Pin 23	J4-11, Shield: J4-44
7	Chan G, Pin 24	J4-10, Shield: J4-43
8	Chan H, Pin 17	J4-17, Shield: J4-50
9	Chan H, Pin 18	J4-16, Shield: J4-49
10	Chan H, Pin 19	J4-15, Shield: J4-48
11	Chan H, Pin 20	J4-14, Shield: J4-47
12	Chan H, Pin 21	J4-13, Shield: J4-46
13	Chan H, Pin 22	J4-12, Shield: J4-45
14	Chan H, Pin 23	J4-11, Shield: J4-44
15	Chan H, Pin 24	J4-10, Shield: J4-43

note: Channel G is on J4-37, shield is on J4-36
Channel H is on J4-35, shield is on J4-34

Register 5Eh (Daughterboard)
Function: Control Matrix pins: 25-32 (channel G, H) for quad 2 X 32
56-64 (channel C, D) for dual 2 X 64
120-128 (channel A, B) for 2 X 128

BIT	FUNCTION	COMMENTS
0	Chan G, Pin 25	J4- 9, Shield: J4-42
1	Chan G, Pin 26	J4- 8, Shield: J4-41
2	Chan G, Pin 27	J4- 7, Shield: J4-40
3	Chan G, Pin 28	J4- 6, Shield: J4-39
4	Chan G, Pin 29	J4- 5, Shield: J4-38
5	Chan G, Pin 30	J4- 4, Shield: J4-36
6	Chan G, Pin 31	J4- 3, Shield: J4-36
7	Chan G, Pin 32	J4- 2, Shield: J4-34
8	Chan G, Pin 25	J4- 9, Shield: J4-42
9	Chan G, Pin 26	J4- 8, Shield: J4-41
10	Chan G, Pin 27	J4- 7, Shield: J4-40
11	Chan G, Pin 28	J4- 6, Shield: J4-39
12	Chan G, Pin 29	J4- 5, Shield: J4-38
13	Chan G, Pin 30	J4- 4, Shield: J4-36
14	Chan G, Pin 31	J4- 3, Shield: J4-36
15	Chan G, Pin 32	J4- 2, Shield: J4-34

note: Channel G is on J4-37, shield is on J4-36
Channel H is on J4-35, shield is on J4-34
Chassis ground is on J4-1