

Model 3000-57

2(4x32) Matrix

90401010



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Regulatory compliance information

This product complies with the essential requirements of the following applicable European Directives, and carries the CE mark accordingly.

89/336/EEC and 73/23/EEC

EN61010-1 (1993)

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Manufacturer's Name:

Giga-tronics, Incorporated

EMC Directive and Low Voltage Directive

Electrical Safety

EMC – Emissions and Immunity

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Type of Equipment:

Switching Module

Model Series Number

3000-57

Declaration of Conformity on file. Contact Giga-tronics at the following;

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TPCI Number	TPCI Issue Date	Date Entered	Comments

Revision History			
Revision	Description of Change	Chg Order #	Approved By
A	Initial Release 1998		
B	Updated		
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Chapter 1 Introduction

1.1 Safety and Manual Conventions

This manual contains conventions regarding safety and equipment usage as described below.

1.1.1 Product Reference

Throughout this manual, the term “Common Core Switching Platform, Series 8800” refers to all models of within the series, unless otherwise specified.

1.1.2 Personal Safety Alert



WARNING: Indicates a hazardous situation which, if not avoided, could result in death or serious injury.

1.1.3 Equipment Safety Alert



CAUTION: Indicates a situation which can damage or adversely affect the product or associated equipment.

1.1.4 Notes

Notes are denoted and used as follows:

NOTE: Highlights or amplifies an essential operating or maintenance procedure, practice, condition or statement.

1.1.5 Electrical Safety Precautions

Any servicing instructions are for use by service-trained personnel only. To avoid personal injury, do not perform any service unless you are qualified to do so.

For continued protections against fire hazard, replace the AC line fuse only with a fuse of the same current rating and type. Do not use repaired fuses or short circuited fuse holders.

Chapter 2 Configuration Table

SINGLE 4X64 TWO WIRE MATRIX

90401010 TOP ASSEMBLY

PL90401010 BOM FOR TOP LEVEL ASSEMBLY

85002830	PWA SUBASSEMBLY (MB)
PL85002830	BOM FOR MB SUBASSEMBLY
SCH85002830	SCHEMATIC FOR MB SUBASSEMBLY
85002840	PWA SUBASSEMBLY (DB)
PL85002840	BOM FOR DB SUBASSEMBLY
SCH85002840	SCHEMATIC FOR DB SUBASSEMBLY

DUAL, 4X32 TWO WIRE MATRIX

90401010001 TOP ASSEMBLY

PL90401010001 BOM FOR TOP LEVEL ASSEMBLY

85002830	PWA SUBASSEMBLY (MB)
PL85002830	BOM FOR MB SUBASSEMBLY
SCH85002830	SCHEMATIC FOR MB SUBASSEMBLY
85002880	PWA SUBASSEMBLY (DB)
PL85002880	BOM FOR DB SUBASSEMBLY
SCH85002880	SCHEMATIC FOR DB SUBASSEMBLY

Chapter 3 Functional Description

3.1 Introduction

This publication provides the necessary information for the maintenance and programming of the Model 3000-57 Switch Matrix. This section provides general information and specifications.

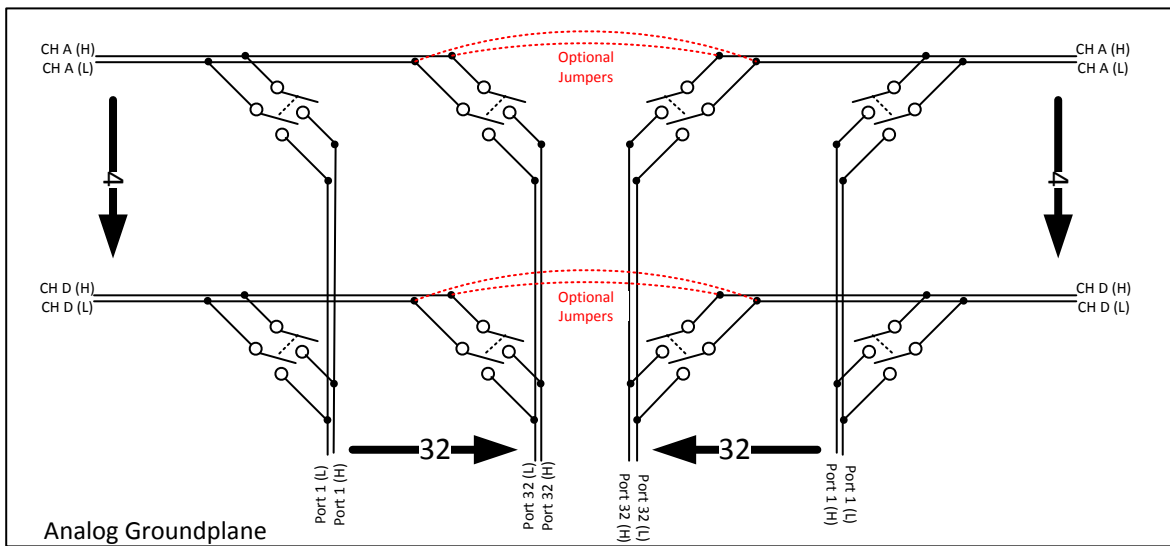
3.2 General Description

This module is a dual wire 4x64 matrix switch. Each relay in the module is individually controlled. Any relay(s) can be closed. The module is designed to support precision testing systems such as ATE (Automatic Testing Equipment). This module is ideal for high quality multi-channel measurement or stimulus switching. Each relay is coaxially shielded to a separate analog ground plane. The Interface and mechanical construction meet the requirements for the VXIbus System Specification, Rev 1.2 through 1.4.

3.3 Functional Description

This module is a universal input/output multi-wire matrix switch. It contains four 4x16 dual wire matrices connected together through isolation relays. Isolation circuits are provided to maintain signal performance by disconnecting unused sections of the matrices.

Chapter 4 Block Diagram

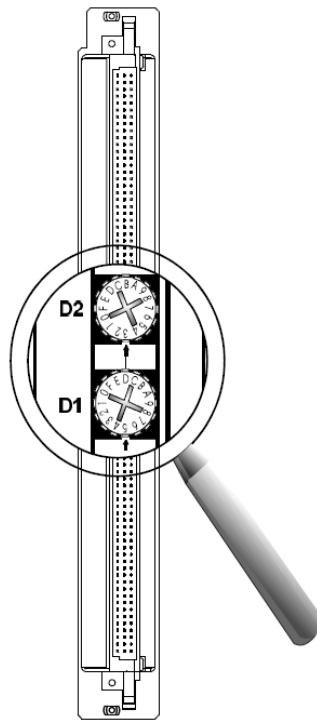


Chapter 5 Controls and Indicators

The following controls and indicators are provided to select and display the functions of the ASCOR 3000-57 Module's operating environment.

5.1 VXI Logical Address

The Logical Address Switch is dual circular switches, D1 and D2 which are located at the rear of the module. The address can be set to any value between 1 and 255 (decimal) or 1 and FF (hexadecimal), (address 0 is reserved for the resource manager). However, the Module fully supports Dynamic Configuration as defined in **Section F of the VXI specification**, address 255 (FF) should be selected only if the Resource Manager also supports Dynamic Configuration.



5.2 LEDs

The following LEDs are visible at the Module's front panel to indicate the status of the module's operation:

5.2.1 "BUS" LED

This green color LED is normally off and will flash on when the module is addressed by the system.

5.2.2 "PWR" LED

This red color LED is normally on when the Module is Powered up.

Chapter 6 Internal Settings

The following items are inside the module and can be reached by removing the side cover.

6.1 Fuse

The ASCOR VXI 3000-57 uses a 10 Amp fuse in the +5 Volt line and is located on the Mother Board (MB) assembly.

6.2 VXI_{bus} Interrupt Level Selection

The VXIbus interrupt level is set with three bits in the “3Eh” register.

See the section on “A16 ADDRESS SPACE REGISTER DESCRIPTION”.

The interrupt level is factory set to “no interrupt”.

Chapter 7 Specifications

Electrical:

Switching Voltage (DC/Peak, AC, Resistive):	220 Volts
Switching Current (DC/Peak, AC, Resistive):	2 Amps
Carry Current (DC/Peak, AC, Resistive):	2 Amps
Contact Power Rating (DC/Peak, AC, Resistive):	60 Watts
Bandwidth:	85 MHz into 50 Ω

Mechanical:

Thickness:	1.200 inches
Width:	10.317 inches
Length:	13.78 inches
Weight:	4 lbs. 10oz.

Environmental Specifications

Temperature:	
Operating:	0° to 55°C
Storage:	- 40° to 75°C
Relative Humidity:	
Operating:	0 to 90% non-condensing
Storage:	0 to 95% non-condensing

Chapter 9 Register Map

9.1 Features

Module register address assignment is controlled by the Resource Manager. The Resource Manager sets the Offset (VXI Configuration) Register at A16 (06h offset) and this defines the A24/A32 Base Address. The unique A24/A32 Base Address is reassigned each time the Resource Manager initiates. This Base Address determines the address of each module register.

You can read the Offset Register at A16 (06h offset) to obtain the A24 Base Address. After reading the Offset Register, map the first (most significant) eight (8) bits of the Offset Register to the first eight (8) bits of the A24 Base Address. To obtain an A32 Base Address, map the first 16 bits of the Offset Register to the first 16 bits of the A32 Base Address. Set all other bits of either Base Address to zeroes.

Alternatively, you can obtain the A24 or A32 Base Address by issuing a library call. See programming Example 1 and Example 2 beginning on page 29.

To obtain the A16 Base Address, use the following formula:

$$\text{A16 Base Address} = \text{C000h} + (\text{Logical Address} \times 40\text{h})$$

Table 9-1. Logical Address and A16 Base Address Relationship

Logical Address	A16 Base Address
1	C040h
2	C080h
3	C0C0h
4	C100h

and so on...

For purposes of interface library calls, the address of each register on the Model 3000-57 is the sum of the following:

- The A24/A32 Base Address.*
- Offset of 8000h or 8020h (motherboard or daughterboard)*
- + The register number minus 1 times 2 or 4 (16-bit or 32-bit address factor); if the register number is 1 then no change*
- = Module register address.*

9.2 Register Programming

The registers that control the motherboard relays start at an offset of 8000h from the A24/A32 Base Address. The registers for the daughterboard start at an offset of 8020h. Module registers can be accessed as either 16-bit words, or 32-bit words. Under 16-bit (D16) mode, address offsets increment by 2h. Under 32-bit (D32) mode, address offsets increment by 4h. Table 9-1 on page 16 shows offsets and bit numbers for both methods.

Table 9-2 on page 18 and Table 9-3 on page 23 list each motherboard or daughterboard relay path connections to the front panel of the card assembly.

In 16-bit mode, each register controls 4 pins at four bits each; in 32-bit mode, each register controls 8 pins. These four bits correspond to the four channels A, B, C, and D. Typically, only one channel is assigned to a pin for optimum performance.

Through your VXI controller, write data to the register in D16 or D32 mode. When a data bit is on (true), the corresponding relay is closed. The state of the relays in a register can be determined by reading the register. The data readback represents the state of the relay coil. This allows you to verify that the program register has correctly controlled the relay coil.

Whenever you close a pin to a channel by setting a bit, the appropriate channel isolation relay must also be closed to complete the path. You close the isolation relay by writing to the last register in the motherboard or daughterboard.

For example, to close pin 1 to channel A and to close pin 2 to channel B, set the following bits:

Register 8000h: Controls pins 1-4.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

Register 8010h: Controls isolation relays.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

For more information on the motherboard and daughterboard devices and locations see Section 4.

Table 9-1. 3000-57 Memory Map

Motherboard Relays

Mode	Offset	Reg #	MSB															Bit Numbers															LSB
16-bit	8000h	1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
32-bit	8000h	1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
Relays Controlled			K16	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1															
16-bit	8002h	2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
32-bit	8000h	1	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16															
Relays Controlled			K32	K31	K30	K29	K28	K27	K26	K25	K24	K23	K22	K21	K20	K19	K18	K17															
16-bit	8004h	3	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
32-bit	8004h	2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
Relays Controlled			K48	K47	K46	K45	K44	K43	K42	K41	K40	K39	K38	K37	K36	K35	K34	K33															
16-bit	8006h	4	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
32-bit	8004h	2	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16															
Relays Controlled			K64	K63	K62	K61	K60	K59	K58	K57	K56	K55	K54	K53	K52	K51	K50	K49															
16-bit	8008h	5	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
32-bit	8008h	3	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
Relays Controlled			K80	K79	K78	K77	K76	K75	K74	K73	K72	K71	K70	K69	K68	K67	K66	K65															
16-bit	800Ah	6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
32-bit	8008h	3	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16															
Relays Controlled			K96	K95	K94	K93	K92	K91	K90	K89	K88	K87	K86	K85	K84	K83	K82	K81															
16-bit	800Ch	7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
32-bit	800Ch	4	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
Relays Controlled			K112	K111	K110	K109	K108	K107	K106	K105	K104	K103	K102	K101	K100	K99	K98	K97															
16-bit	800Eh	8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
32-bit	800Ch	4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16															
Relays Controlled			K128	K127	K126	K125	K124	K123	K122	K121	K120	K119	K118	K117	K116	K115	K114	K113															
16-bit	8010h	9	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
32-bit	8010h	5	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0															
Relays Controlled			—	—	—	—	—	—	—	—	K136	K135	K134	K133	K132	K131	K130	K129															

Table 9-1. 3000-57 Memory Map, Continued

Daughterboard Relays																		
16-bit	8020h	10	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
32-bit	8020h	6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Relays Controlled			K16	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1
16-bit	8022h	11	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
32-bit	8020h	6	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Relays Controlled			K32	K31	K30	K29	K28	K27	K26	K25	K24	K23	K22	K21	K20	K19	K18	K17
16-bit	8024h	12	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
32-bit	8024h	7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Relays Controlled			K48	K47	K46	K45	K44	K43	K42	K41	K40	K39	K38	K37	K36	K35	K34	K33
16-bit	8026h	13	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
32-bit	8024h	7	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Relays Controlled			K64	K63	K62	K61	K60	K59	K58	K57	K56	K55	K54	K53	K52	K51	K50	K49
16-bit	8028h	14	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
32-bit	8028h	8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Relays Controlled			K80	K79	K78	K77	K76	K75	K74	K73	K72	K71	K70	K69	K68	K67	K66	K65
16-bit	802Ah	15	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
32-bit	8028h	8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Relays Controlled			K96	K95	K94	K93	K92	K91	K90	K89	K88	K87	K86	K85	K84	K83	K82	K81
16-bit	802Ch	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
32-bit	802Ch	9	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Relays Controlled			K112	K111	K110	K109	K108	K107	K106	K105	K104	K103	K102	K101	K100	K99	K98	K97
16-bit	802Eh	17	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
32-bit	802Ch	9	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Relays Controlled			K128	K127	K126	K125	K124	K123	K122	K121	K120	K119	K118	K117	K116	K115	K114	K113
16-bit	8030h	18	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
32-bit	8030h	10	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Relays Controlled			—	—	—	—	—	—	—	—	K136	K135	K134	K133	K132	K131	K130	K129

Table 9-2. Relays, Motherboard, PCB SCH85002830

Mode: Offset :	16-bit 8000h	32-bit 8000h	Description: Control matrix pins 1–4, Channels A, B, C, and D.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K1	0	0	Channel A, Pin 1.	J1-50, 49, 48. Channel A is J2-35, 36, 34.
K2	1	1	Channel B, Pin 1.	J1-50, 49, 48. Channel B is J2-32, 33, 31.
K3	2	2	Channel C, Pin 1.	J1-50, 49, 48. Channel C is J2-5, 6, 4.
K4	3	3	Channel D, Pin 1.	J1-50, 49, 48. Channel D is J2-2, 3, 1.
K5	4	4	Channel A, Pin 2.	J1-25, 24, 23. Channel A is J2-35, 36, 34.
K6	5	5	Channel B, Pin 2.	J1-25, 24, 23. Channel B is J2-32, 33, 31.
K7	6	6	Channel C, Pin 2.	J1-25, 24, 23. Channel C is J2-5, 6, 4.
K8	7	7	Channel D, Pin 2.	J1-25, 24, 23. Channel D is J2-2, 3, 1.
K9	8	8	Channel A, Pin 3.	J1-47, 46, 45. Channel A is J2-35, 36, 34.
K10	9	9	Channel B, Pin 3.	J1-47, 46, 45. Channel B is J2-32, 33, 31.
K11	10	10	Channel C, Pin 3.	J1-47, 46, 45. Channel C is J2-5, 6, 4.
K12	11	11	Channel D, Pin 3.	J1-47, 46, 45. Channel D is J2-2, 3, 1.
K13	12	12	Channel A, Pin 4.	J1-22, 21, 20. Channel A is J2-35, 36, 34.
K14	13	13	Channel B, Pin 4.	J1-22, 21, 20. Channel B is J2-32, 33, 31.
K15	14	14	Channel C, Pin 4.	J1-22, 21, 20. Channel C is J2-5, 6, 4.
K16	15	15	Channel D, Pin 4.	J1-22, 21, 20. Channel D is J2-2, 3, 1.
Mode: Offset :	16-bit 8002h	32-bit 8000h	Description: Control matrix pins 5–8, Channels A, B, C, and D.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K17	0	16	Channel A, Pin 5.	J1-44, 43, 42. Channel A is J2-35, 36, 34.
K18	1	17	Channel B, Pin 5.	J1-44, 43, 42. Channel B is J2-32, 33, 31.
K19	2	18	Channel C, Pin 5.	J1-44, 43, 42. Channel C is J2-5, 6, 4.
K20	3	19	Channel D, Pin 5.	J1-44, 43, 42. Channel D is J2-2, 3, 1.
K21	4	20	Channel A, Pin 6.	J1-19, 18, 17. Channel A is J2-35, 36, 34.
K22	5	21	Channel B, Pin 6.	J1-19, 18, 17. Channel B is J2-32, 33, 31.
K23	6	22	Channel C, Pin 6.	J1-19, 18, 17. Channel C is J2-5, 6, 4.
K24	7	23	Channel D, Pin 6.	J1-19, 18, 17. Channel D is J2-2, 3, 1.
K25	8	24	Channel A, Pin 7.	J1-41, 40, 39. Channel A is J2-35, 36, 34.
K26	9	25	Channel B, Pin 7.	J1-41, 40, 39. Channel B is J2-32, 33, 31.
K27	10	26	Channel C, Pin 7.	J1-41, 40, 39. Channel C is J2-5, 6, 4.
K28	11	27	Channel D, Pin 7.	J1-41, 40, 39. Channel D is J2-2, 3, 1.
K29	12	28	Channel A, Pin 8.	J1-16, 15, 14. Channel A is J2-35, 36, 34.
K30	13	29	Channel B, Pin 8.	J1-16, 15, 14. Channel B is J2-32, 33, 31.
K31	14	30	Channel C, Pin 8.	J1-16, 15, 14. Channel C is J2-5, 6, 4.
K32	15	31	Channel D, Pin 8.	J1-16, 15, 14. Channel D is J2-2, 3, 1.

Table 9-2. Relays, Motherboard, PCB sch85002830, *Continued*

Mode: Offset :	16-bit 8004h	32-bit 8004h	Description: Control matrix pins 9–12, Channels A, B, C, and D.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K33	0	0	Channel A, Pin 9.	J1-38, 37, 36. Channel A is J2-35, 36, 34.
K34	1	1	Channel B, Pin 9.	J1-38, 37, 36. Channel B is J2-32, 33, 31.
K35	2	2	Channel C, Pin 9.	J1-38, 37, 36. Channel C is J2-5, 6, 4.
K36	3	3	Channel D, Pin 9.	J1-38, 37, 36. Channel D is J2-2, 3, 1.
K37	4	4	Channel A, Pin 10.	J1-13, 12, 11. Channel A is J2-35, 36, 34.
K38	5	5	Channel B, Pin 10.	J1-13, 12, 11. Channel B is J2-32, 33, 31.
K39	6	6	Channel C, Pin 10.	J1-13, 12, 11. Channel C is J2-5, 6, 4.
K40	7	7	Channel D, Pin 10.	J1-13, 12, 11. Channel D is J2-2, 3, 1.
K41	8	8	Channel A, Pin 11.	J1-35, 34, 33. Channel A is J2-35, 36, 34.
K42	9	9	Channel B, Pin 11.	J1-35, 34, 33. Channel B is J2-32, 33, 31.
K43	10	10	Channel C, Pin 11.	J1-35, 34, 33. Channel C is J2-5, 6, 4.
K44	11	11	Channel D, Pin 11.	J1-35, 34, 33. Channel D is J2-2, 3, 1.
K45	12	12	Channel A, Pin 12.	J1-10, 9, 8. Channel A is J2-35, 36, 34.
K46	13	13	Channel B, Pin 12.	J1-10, 9, 8. Channel B is J2-32, 33, 31.
K47	14	14	Channel C, Pin 12.	J1-10, 9, 8. Channel C is J2-5, 6, 4.
K48	15	15	Channel D, Pin 12.	J1-10, 9, 8. Channel D is J2-2, 3, 1.
Mode: Offset :	16-bit 8006h	32-bit 8004h	Description: Control matrix pins 13–16, Channels A, B, C, and D.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K49	0	16	Channel A, Pin 13.	J1-32, 31, 30. Channel A is J2-35, 36, 34.
K50	1	17	Channel B, Pin 13.	J1-32, 31, 30. Channel B is J2-32, 33, 31.
K51	2	18	Channel C, Pin 13.	J1-32, 31, 30. Channel C is J2-5, 6, 4.
K52	3	19	Channel D, Pin 13.	J1-32, 31, 30. Channel D is J2-2, 3, 1.
K53	4	20	Channel A, Pin 14.	J1-7, 6, 5. Channel A is J2-35, 36, 34.
K54	5	21	Channel B, Pin 14.	J1-7, 6, 5. Channel B is J2-32, 33, 31.
K55	6	22	Channel C, Pin 14.	J1-7, 6, 5. Channel C is J2-5, 6, 4.
K56	7	23	Channel D, Pin 14.	J1-7, 6, 5. Channel D is J2-2, 3, 1.
K57	8	24	Channel A, Pin 15.	J1-29, 28, 27. Channel A is J2-35, 36, 34.
K58	9	25	Channel B, Pin 15.	J1-29, 28, 27. Channel B is J2-32, 33, 31.
K59	10	26	Channel C, Pin 15.	J1-29, 28, 27. Channel C is J2-5, 6, 4.
K60	11	27	Channel D, Pin 15.	J1-29, 28, 27. Channel D is J2-2, 3, 1.
K61	12	28	Channel A, Pin 16.	J1-4, 3, 2. Channel A is J2-35, 36, 34.
K62	13	29	Channel B, Pin 16.	J1-4, 3, 2. Channel B is J2-32, 33, 31.
K63	14	30	Channel C, Pin 16.	J1-4, 3, 2. Channel C is J2-5, 6, 4.
K64	15	31	Channel D, Pin 16.	J1-4, 3, 2. Channel D is J2-2, 3, 1.

Table 9-2. Relays, Motherboard, PCB sch85002830, *Continued*

Mode: Offset :	16-bit 8008h	32-bit 8008h	Description: Control matrix pins 17–20, Channels A, B, C, and D.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K65	0	0	Channel A, Pin 17.	J2-60, 59, 58. Channel A is J2-35, 36, 34.
K66	1	1	Channel B, Pin 17.	J2-60, 59, 58. Channel B is J2-32, 33, 31.
K67	2	2	Channel C, Pin 17.	J2-60, 59, 58. Channel C is J2-5, 6, 4.
K68	3	3	Channel D, Pin 17.	J2-60, 59, 58. Channel D is J2-2, 3, 1.
K69	4	4	Channel A, Pin 18.	J2-30, 29, 28. Channel A is J2-35, 36, 34.
K70	5	5	Channel B, Pin 18.	J2-30, 29, 28. Channel B is J2-32, 33, 31.
K71	6	6	Channel C, Pin 18.	J2-30, 29, 28. Channel C is J2-5, 6, 4.
K72	7	7	Channel D, Pin 18.	J2-30, 29, 28. Channel D is J2-2, 3, 1.
K73	8	8	Channel A, Pin 19.	J2-57, 56, 55. Channel A is J2-35, 36, 34.
K74	9	9	Channel B, Pin 19.	J2-57, 56, 55. Channel B is J2-32, 33, 31.
K75	10	10	Channel C, Pin 19.	J2-57, 56, 55. Channel C is J2-5, 6, 4.
K76	11	11	Channel D, Pin 19.	J2-57, 56, 55. Channel D is J2-2, 3, 1.
K77	12	12	Channel A, Pin 20.	J2-27, 26, 25. Channel A is J2-35, 36, 34.
K78	13	13	Channel B, Pin 20.	J2-27, 26, 25. Channel B is J2-32, 33, 31.
K79	14	14	Channel C, Pin 20.	J2-27, 26, 25. Channel C is J2-5, 6, 4.
K80	15	15	Channel D, Pin 20.	J2-27, 26, 25. Channel D is J2-2, 3, 1.
Mode: Offset :	16-bit 800A h	32-bit 8008h	Description: Control matrix pins 21–24, Channels A, B, C, and D.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K81	0	16	Channel A, Pin 21.	J2-54, 53, 52. Channel A is J2-35, 36, 34.
K82	1	17	Channel B, Pin 21.	J2-54, 53, 52. Channel B is J2-32, 33, 31.
K83	2	18	Channel C, Pin 21.	J2-54, 53, 52. Channel C is J2-5, 6, 4.
K84	3	19	Channel D, Pin 21.	J2-54, 53, 52. Channel D is J2-2, 3, 1.
K85	4	20	Channel A, Pin 22.	J2-24, 23, 22. Channel A is J2-35, 36, 34.
K86	5	21	Channel B, Pin 22.	J2-24, 23, 22. Channel B is J2-32, 33, 31.
K87	6	22	Channel C, Pin 22.	J2-24, 23, 22. Channel C is J2-5, 6, 4.
K88	7	23	Channel D, Pin 22.	J2-24, 23, 22. Channel D is J2-2, 3, 1.
K89	8	24	Channel A, Pin 23.	J2-51, 50, 49. Channel A is J2-35, 36, 34.
K90	9	25	Channel B, Pin 23.	J2-51, 50, 49. Channel B is J2-32, 33, 31.
K91	10	26	Channel C, Pin 23.	J2-51, 50, 49. Channel C is J2-5, 6, 4.
K92	11	27	Channel D, Pin 23.	J2-51, 50, 49. Channel D is J2-2, 3, 1.
K93	12	28	Channel A, Pin 24.	J2-21, 20, 19. Channel A is J2-35, 36, 34.
K94	13	29	Channel B, Pin 24.	J2-21, 20, 19. Channel B is J2-32, 33, 31.
K95	14	30	Channel C, Pin 24.	J2-21, 20, 19. Channel C is J2-5, 6, 4.
K96	15	31	Channel D, Pin 24.	J2-21, 20, 19. Channel D is J2-2, 3, 1.

Table 9-2. Relays, Motherboard, PCB sch85002830, *Continued*

Mode: Offset :	16-bit 800C h	32-bit 800C h	Description: Control matrix pins 25–28, Channels A, B, C, and D.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K97	0	0	Channel A, Pin 25.	J2-48, 47, 46. Channel A is J2-35, 36, 34.
K98	1	1	Channel B, Pin 25.	J2-48, 47, 46. Channel B is J2-32, 33, 31.
K99	2	2	Channel C, Pin 25.	J2-48, 47, 46. Channel C is J2-5, 6, 4.
K100	3	3	Channel D, Pin 25.	J2-48, 47, 46. Channel D is J2-2, 3, 1.
K101	4	4	Channel A, Pin 26.	J2-18, 17, 16. Channel A is J2-35, 36, 34.
K102	5	5	Channel B, Pin 26.	J2-18, 17, 16. Channel B is J2-32, 33, 31.
K103	6	6	Channel C, Pin 26.	J2-18, 17, 16. Channel C is J2-5, 6, 4.
K104	7	7	Channel D, Pin 26.	J2-18, 17, 16. Channel D is J2-2, 3, 1.
K105	8	8	Channel A, Pin 27.	J2-45, 44, 43. Channel A is J2-35, 36, 34.
K106	9	9	Channel B, Pin 27.	J2-45, 44, 43. Channel B is J2-32, 33, 31.
K107	10	10	Channel C, Pin 27.	J2-45, 44, 43. Channel C is J2-5, 6, 4.
K108	11	11	Channel D, Pin 27.	J2-45, 44, 43. Channel D is J2-2, 3, 1.
K109	12	12	Channel A, Pin 28.	J2-15, 14, 13. Channel A is J2-35, 36, 34.
K110	13	13	Channel B, Pin 28.	J2-15, 14, 13. Channel B is J2-32, 33, 31.
K111	14	14	Channel C, Pin 28.	J2-15, 14, 13. Channel C is J2-5, 6, 4.
K112	15	15	Channel D, Pin 28.	J2-15, 14, 13. Channel D is J2-2, 3, 1.
Mode: Offset :	16-bit 800E h	32-bit 800C h	Description: Control matrix pins 29–32, Channels A, B, C, and D.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K113	0	16	Channel A, Pin 29.	J2-42, 41, 40. Channel A is J2-35, 36, 34.
K114	1	17	Channel B, Pin 29.	J2-42, 41, 40. Channel B is J2-32, 33, 31.
K115	2	18	Channel C, Pin 29.	J2-42, 41, 40. Channel C is J2-5, 6, 4.
K116	3	19	Channel D, Pin 29.	J2-42, 41, 40. Channel D is J2-2, 3, 1.
K117	4	20	Channel A, Pin 30.	J2-12, 11, 10. Channel A is J2-35, 36, 34.
K118	5	21	Channel B, Pin 30.	J2-12, 11, 10. Channel B is J2-32, 33, 31.
K119	6	22	Channel C, Pin 30.	J2-12, 11, 10. Channel C is J2-5, 6, 4.
K120	7	23	Channel D, Pin 30.	J2-12, 11, 10. Channel D is J2-2, 3, 1.
K121	8	24	Channel A, Pin 31.	J2-39, 38, 37. Channel A is J2-35, 36, 34.
K122	9	25	Channel B, Pin 31.	J2-39, 38, 37. Channel B is J2-32, 33, 31.
K123	10	26	Channel C, Pin 31.	J2-39, 38, 37. Channel C is J2-5, 6, 4.
K124	11	27	Channel D, Pin 31.	J2-39, 38, 37. Channel D is J2-2, 3, 1.
K125	12	28	Channel A, Pin 32.	J2-9, 8, 7. Channel A is J2-35, 36, 34.
K126	13	29	Channel B, Pin 32.	J2-9, 8, 7. Channel B is J2-32, 33, 31.
K127	14	30	Channel C, Pin 32.	J2-9, 8, 7. Channel C is J2-5, 6, 4.
K128	15	31	Channel D, Pin 32.	J2-9, 8, 7. Channel D is J2-2, 3, 1.

Table 9-2. Relays, Motherboard, PCB sch85002830, *Continued*

Mode: Offset :	16-bit 8010h	32-bit 8010h	Definition: Control matrix isolation relays, Channels A, B, C, and D.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
<i>K129</i>	0	0	Isolation Channel A, Group 1.	J2-35, 36, 34.
<i>K130</i>	1	1	Isolation Channel B, Group 1.	J2-32, 33, 31.
<i>K131</i>	2	2	Isolation Channel C, Group 1.	J2-5, 6, 4.
<i>K132</i>	3	3	Isolation Channel D, Group 1.	J2-2, 3, 1.
<i>K133</i>	4	4	Isolation Channel A, Group 2.	J2-35, 36, 34.
<i>K134</i>	5	5	Isolation Channel B, Group 2.	J2-32, 33, 31.
<i>K135</i>	6	6	Isolation Channel C, Group 2.	J2-5, 6, 4.
<i>K136</i>	7	7	Isolation Channel D, Group 2.	J2-2, 3, 1.
—	8	8	Not used.	Not used.
—	9	9	Not used.	Not used.
—	10	10	Not used.	Not used.
—	11	11	Not used.	Not used.
—	12	12	Not used.	Not used.
—	13	13	Not used.	Not used.
—	14	14	Not used.	Not used.
—	15	15	Not used.	Not used.

Table 9-3. Relays, Daughterboard, PCB sch85002880

Mode: Offset :	16-bit 8020h	32-bit 8020h	Description: Control matrix pins 33-36, Channels A, B, C, and D, Daughterboard #1.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K1	0	0	Channel A, Pin 33.	J3-50, 49, 48. Channel A is J2-35, 36, 34.
K2	1	1	Channel B, Pin 33.	J3-50, 49, 48. Channel B is J2-32, 33, 31.
K3	2	2	Channel C, Pin 33.	J3-50, 49, 48. Channel C is J2-5, 6, 4.
K4	3	3	Channel D, Pin 33.	J3-50, 49, 48. Channel D is J2-2, 3, 1.
K5	4	4	Channel A, Pin 34.	J3-25, 24, 23. Channel A is J2-35, 36, 34.
K6	5	5	Channel B, Pin 34.	J3-25, 24, 23. Channel B is J2-32, 33, 31.
K7	6	6	Channel C, Pin 34.	J3-25, 24, 23. Channel C is J2-5, 6, 4.
K8	7	7	Channel D, Pin 34.	J3-25, 24, 23. Channel D is J2-2, 3, 1.
K9	8	8	Channel A, Pin 35.	J3-47, 46, 45. Channel A is J2-35, 36, 34.
K10	9	9	Channel B, Pin 35.	J3-47, 46, 45. Channel B is J2-32, 33, 31.
K11	10	10	Channel C, Pin 35.	J3-47, 46, 45. Channel C is J2-5, 6, 4.
K12	11	11	Channel D, Pin 35.	J3-47, 46, 45. Channel D is J2-2, 3, 1.
K13	12	12	Channel A, Pin 36.	J3-22, 21, 20. Channel A is J2-35, 36, 34.
K14	13	13	Channel B, Pin 36.	J3-22, 21, 20. Channel B is J2-32, 33, 31.
K15	14	14	Channel C, Pin 36.	J3-22, 21, 20. Channel C is J2-5, 6, 4.
K16	15	15	Channel D, Pin 36.	J3-22, 21, 20. Channel D is J2-2, 3, 1.
Mode: Offset :	16-bit 8022h	32-bit 8020h	Description: Control matrix pins 37-40, Channels A, B, C, and D, Daughterboard #1.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K17	0	16	Channel A, Pin 37.	J3-44, 43, 42. Channel A is J2-35, 36, 34.
K18	1	17	Channel B, Pin 37.	J3-44, 43, 42. Channel B is J2-32, 33, 31.
K19	2	18	Channel C, Pin 37.	J3-44, 43, 42. Channel C is J2-5, 6, 4.
K20	3	19	Channel D, Pin 37.	J3-44, 43, 42. Channel D is J2-2, 3, 1.
K21	4	20	Channel A, Pin 38.	J3-19, 18, 17. Channel A is J2-35, 36, 34.
K22	5	21	Channel B, Pin 38.	J3-19, 18, 17. Channel B is J2-32, 33, 31.
K23	6	22	Channel C, Pin 38.	J3-19, 18, 17. Channel C is J2-5, 6, 4.
K24	7	23	Channel D, Pin 38.	J3-19, 18, 17. Channel D is J2-2, 3, 1.
K25	8	24	Channel A, Pin 39.	J3-41, 40, 39. Channel A is J2-35, 36, 34.
K26	9	25	Channel B, Pin 39.	J3-41, 40, 39. Channel B is J2-32, 33, 31.
K27	10	26	Channel C, Pin 39.	J3-41, 40, 39. Channel C is J2-5, 6, 4.
K28	11	27	Channel D, Pin 39.	J3-41, 40, 39. Channel D is J2-2, 3, 1.
K29	12	28	Channel A, Pin 40.	J3-16, 15, 14. Channel A is J2-35, 36, 34.
K30	13	29	Channel B, Pin 40.	J3-16, 15, 14. Channel B is J2-32, 33, 31.
K31	14	30	Channel C, Pin 40.	J3-16, 15, 14. Channel C is J2-5, 6, 4.
K32	15	31	Channel D, Pin 40.	J3-16, 15, 14. Channel D is J2-2, 3, 1.

Table 9-3. Relays, Daughterboard, PCB SCH85002880,

Continued

Mode: Offset :	16-bit 8024h	32-bit 8024h	Description: Control matrix: 41-44, Channels A, B, C, and D, Daughterboard #1.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K33	0	0	Channel A, Pin 41.	J3-38, 37, 36. Channel A is J2-35, 36, 34.
K34	1	1	Channel B, Pin 41.	J3-38, 37, 36. Channel B is J2-32, 33, 31.
K35	2	2	Channel C, Pin 41.	J3-38, 37, 36. Channel C is J2-5, 6, 4.
K36	3	3	Channel D, Pin 41.	J3-38, 37, 36. Channel D is J2-2, 3, 1.
K37	4	4	Channel A, Pin 42.	J3-13, 12, 11. Channel A is J2-35, 36, 34.
K38	5	5	Channel B, Pin 42.	J3-13, 12, 11. Channel B is J2-32, 33, 31.
K39	6	6	Channel C, Pin 42.	J3-13, 12, 11. Channel C is J2-5, 6, 4.
K40	7	7	Channel D, Pin 42.	J3-13, 12, 11. Channel D is J2-2, 3, 1.
K41	8	8	Channel A, Pin 43.	J3-35, 34, 33. Channel A is J2-35, 36, 34.
K42	9	9	Channel B, Pin 43.	J3-35, 34, 33. Channel B is J2-32, 33, 31.
K43	10	10	Channel C, Pin 43.	J3-35, 34, 33. Channel C is J2-5, 6, 4.
K44	11	11	Channel D, Pin 43.	J3-35, 34, 33. Channel D is J2-2, 3, 1.
K45	12	12	Channel A, Pin 44.	J3-10, 9, 8. Channel A is J2-35, 36, 34.
K46	13	13	Channel B, Pin 44.	J3-10, 9, 8. Channel B is J2-32, 33, 31.
K47	14	14	Channel C, Pin 44.	J3-10, 9, 8. Channel C is J2-5, 6, 4.
K48	15	15	Channel D, Pin 44.	J3-10, 9, 8. Channel D is J2-2, 3, 1.
Mode: Offset :	16-bit 8026h	32-bit 8024h	Description: Control matrix: pins 45-48, Channels A, B, C, and D, Daughterboard #1.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K49	0	16	Channel A, Pin 45.	J3-32, 31, 30. Channel A is J2-35, 36, 34.
K50	1	17	Channel B, Pin 45.	J3-32, 31, 30. Channel B is J2-32, 33, 31.
K51	2	18	Channel C, Pin 45.	J3-32, 31, 30. Channel C is J2-5, 6, 4.
K52	3	19	Channel D, Pin 45.	J3-32, 31, 30. Channel D is J2-2, 3, 1.
K53	4	20	Channel A, Pin 46.	J3-7, 6, 5. Channel A is J2-35, 36, 34.
K54	5	21	Channel B, Pin 46.	J3-7, 6, 5. Channel B is J2-32, 33, 31.
K55	6	22	Channel C, Pin 46.	J3-7, 6, 5. Channel C is J2-5, 6, 4.
K56	7	23	Channel D, Pin 46.	J3-7, 6, 5. Channel D is J2-2, 3, 1.
K57	8	24	Channel A, Pin 47.	J3-29, 28, 27. Channel A is J2-35, 36, 34.
K58	9	25	Channel B, Pin 47.	J3-29, 28, 27. Channel B is J2-32, 33, 31.
K59	10	26	Channel C, Pin 47.	J3-29, 28, 27. Channel C is J2-5, 6, 4.
K60	11	27	Channel D, Pin 47.	J3-29, 28, 27. Channel D is J2-2, 3, 1.
K61	12	28	Channel A, Pin 48.	J3-4, 3, 2. Channel A is J2-35, 36, 34.
K62	13	29	Channel B, Pin 48.	J3-4, 3, 2. Channel B is J2-32, 33, 31.
K63	14	30	Channel C, Pin 48.	J3-4, 3, 2. Channel C is J2-5, 6, 4.
K64	15	31	Channel D, Pin 48.	J3-4, 3, 2. Channel D is J2-2, 3, 1.

Table 9-3. Relays, Daughterboard, PCB SCH85002880,

Continued

Mode: Offset :	16-bit 8028h	32-bit 8028h	Description: Control matrix: 49-52, Channels A, B, C, and D, Daughterboard #1.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K65	0	0	Channel A, Pin 49.	J4-50, 49, 48. Channel A is J2-35, 36, 34.
K66	1	1	Channel B, Pin 49.	J4-50, 49, 48. Channel B is J2-32, 33, 31.
K67	2	2	Channel C, Pin 49.	J4-50, 49, 48. Channel C is J2-5, 6, 4.
K68	3	3	Channel D, Pin 49.	J4-50, 49, 48. Channel D is J2-2, 3, 1.
K69	4	4	Channel A, Pin 50.	J4-25, 24, 23. Channel A is J2-35, 36, 34.
K70	5	5	Channel B, Pin 50.	J4-25, 24, 23. Channel B is J2-32, 33, 31.
K71	6	6	Channel C, Pin 50.	J4-25, 24, 23. Channel C is J2-5, 6, 4.
K72	7	7	Channel D, Pin 50.	J4-25, 24, 23. Channel D is J2-2, 3, 1.
K73	8	8	Channel A, Pin 51.	J4-47, 46, 45. Channel A is J2-35, 36, 34.
K74	9	9	Channel B, Pin 51.	J4-47, 46, 45. Channel B is J2-32, 33, 31.
K75	10	10	Channel C, Pin 51.	J4-47, 46, 45. Channel C is J2-5, 6, 4.
K76	11	11	Channel D, Pin 51.	J4-47, 46, 45. Channel D is J2-2, 3, 1.
K77	12	12	Channel A, Pin 52.	J4-22, 21, 20. Channel A is J2-35, 36, 34.
K78	13	13	Channel B, Pin 52.	J4-22, 21, 20. Channel B is J2-32, 33, 31.
K79	14	14	Channel C, Pin 52.	J4-22, 21, 20. Channel C is J2-5, 6, 4.
K80	15	15	Channel D, Pin 52.	J4-22, 21, 20. Channel D is J2-2, 3, 1.
Mode: Offset :	16-bit 802A h	32-bit 8028h	Description: Control matrix: pins 53-56, Channels A, B, C, and D, Daughterboard #1.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K81	0	16	Channel A, Pin 53.	J4-44, 43, 42. Channel A is J2-35, 36, 34.
K82	1	17	Channel B, Pin 53.	J4-54, 53, 52. Channel B is J2-32, 33, 31.
K83	2	18	Channel C, Pin 53.	J4-44, 43, 42. Channel C is J2-5, 6, 4.
K84	3	19	Channel D, Pin 53.	J4-44, 43, 42. Channel D is J2-2, 3, 1.
K85	4	20	Channel A, Pin 54.	J4-19, 18, 17. Channel A is J2-35, 36, 34.
K86	5	21	Channel B, Pin 54.	J4-19, 18, 17. Channel B is J2-32, 33, 31.
K87	6	22	Channel C, Pin 54.	J4-19, 18, 17. Channel C is J2-5, 6, 4.
K88	7	23	Channel D, Pin 54.	J4-19, 18, 17. Channel D is J2-2, 3, 1.
K89	8	24	Channel A, Pin 55.	J4-41, 40, 39. Channel A is J2-35, 36, 34.
K90	9	25	Channel B, Pin 55.	J4-41, 40, 39. Channel B is J2-32, 33, 31.
K91	10	26	Channel C, Pin 55.	J4-41, 40, 39. Channel C is J2-5, 6, 4.
K92	11	27	Channel D, Pin 55.	J4-41, 40, 39. Channel D is J2-2, 3, 1.
K93	12	28	Channel A, Pin 56.	J4-16, 15, 14. Channel A is J2-35, 36, 34.
K94	13	29	Channel B, Pin 56.	J4-16, 15, 14. Channel B is J2-32, 33, 31.
K95	14	30	Channel C, Pin 56.	J4-16, 15, 14. Channel C is J2-5, 6, 4.
K96	15	31	Channel D, Pin 56.	J4-16, 15, 14. Channel D is J2-2, 3, 1.

Table 9-3. Relays, Daughterboard, PCB SCH85002880,

Continued

Mode: Offset :	16-bit 802C h	32-bit 802C h	Description: Control matrix: 57-60, Channels A, B, C, and D, Daughterboard #1.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K97	0	0	Channel A, Pin 57.	J4-38, 37, 36. Channel A is J2-35, 36, 34.
K98	1	1	Channel B, Pin 57.	J4-38, 37, 36. Channel B is J2-32, 33, 31.
K99	2	2	Channel C, Pin 57.	J4-38, 37, 36. Channel C is J2-5, 6, 4.
K100	3	3	Channel D, Pin 57.	J4-38, 37, 36. Channel D is J2-2, 3, 1.
K101	4	4	Channel A, Pin 58.	J4-13, 12, 11. Channel A is J2-35, 36, 34.
K102	5	5	Channel B, Pin 58.	J4-13, 12, 11. Channel B is J2-32, 33, 31.
K103	6	6	Channel C, Pin 58.	J4-13, 12, 11. Channel C is J2-5, 6, 4.
K104	7	7	Channel D, Pin 58.	J4-13, 12, 11. Channel D is J2-2, 3, 1.
K105	8	8	Channel A, Pin 59.	J4-35, 34, 33. Channel A is J2-35, 36, 34.
K106	9	9	Channel B, Pin 59.	J4-35, 34, 33. Channel B is J2-32, 33, 31.
K107	10	10	Channel C, Pin 59.	J4-35, 34, 33. Channel C is J2-5, 6, 4.
K108	11	11	Channel D, Pin 59.	J4-35, 34, 33. Channel D is J2-2, 3, 1.
K109	12	12	Channel A, Pin 60.	J4-10, 9, 8. Channel A is J2-35, 36, 34.
K110	13	13	Channel B, Pin 60.	J4-10, 9, 8. Channel B is J2-32, 33, 31.
K111	14	14	Channel C, Pin 60.	J4-10, 9, 8. Channel C is J2-5, 6, 4.
K112	15	15	Channel D, Pin 60.	J4-10, 9, 8. Channel D is J2-2, 3, 1.
Mode: Offset :	16-bit 802E h	32-bit 802C h	Description: Control matrix: pins 61-64, Channels A, B, C, and D, Daughterboard #1.	
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K113	0	16	Channel A, Pin 61.	J4-32, 31, 30. Channel A is J2-35, 36, 34.
K114	1	17	Channel B, Pin 61.	J4-32, 31, 30. Channel B is J2-32, 33, 31.
K115	2	18	Channel C, Pin 61.	J4-32, 31, 30. Channel C is J2-5, 6, 4.
K116	3	19	Channel D, Pin 61.	J4-32, 31, 30. Channel D is J2-2, 3, 1.
K117	4	20	Channel A, Pin 62.	J4-7, 6, 5. Channel A is J2-35, 36, 34.
K118	5	21	Channel B, Pin 62.	J4-7, 6, 5. Channel B is J2-32, 33, 31.
K119	6	22	Channel C, Pin 62.	J4-7, 6, 5. Channel C is J2-5, 6, 4.
K120	7	23	Channel D, Pin 62.	J4-7, 6, 5. Channel D is J2-2, 3, 1.
K121	8	24	Channel A, Pin 63.	J4-29, 28, 27. Channel A is J2-35, 36, 34.
K122	9	25	Channel B, Pin 63.	J4-29, 28, 27. Channel B is J2-32, 33, 31.
K123	10	26	Channel C, Pin 63.	J4-29, 28, 27. Channel C is J2-5, 6, 4.
K124	11	27	Channel D, Pin 63.	J4-29, 28, 27. Channel D is J2-2, 3, 1.
K125	12	28	Channel A, Pin 64.	J4-4, 3, 2. Channel A is J2-35, 36, 34.
K126	13	29	Channel B, Pin 64.	J4-4, 3, 2. Channel B is J2-32, 33, 31.
K127	14	30	Channel C, Pin 64.	J4-4, 3, 2. Channel C is J2-5, 6, 4.
K128	15	31	Channel D, Pin 64.	J4-4, 3, 2. Channel D is J2-2, 3, 1.

Table 9-3. Relays, Daughterboard, PCB SCH85002880,

Continued

Mode:	16-bit	32-bit	Definition: <i>Control matrix: isolation relays, Channels A, B, C, and D, Daughterboard #1.</i>	
Offset	8030h	8030h		
:				
Relay #	Bit	Bit	Function	Connection (H, L, Shield)
K129	0	0	Isolation Channel A, Group 1.	J2-35, 36, 34.
K130	1	1	Isolation Channel B, Group 1.	J2-32, 33, 31.
K131	2	2	Isolation Channel C, Group 1.	J2-5, 6, 4.
K132	3	3	Isolation Channel D, Group 1.	J2-2, 3, 1.
K133	4	4	Isolation Channel A, Group 2.	J2-35, 36, 34.
K134	5	5	Isolation Channel B, Group 2.	J2-32, 33, 31.
K135	6	6	Isolation Channel C, Group 2.	J2-5, 6, 4.
K136	7	7	Isolation Channel D, Group 2.	J2-2, 3, 1.
—	8	8	Not used.	Not used.
—	9	9	Not used.	Not used.
—	10	10	Not used.	Not used.
—	11	11	Not used.	Not used.
—	12	12	Not used.	Not used.
—	13	13	Not used.	Not used.
—	14	14	Not used.	Not used.
—	15	15	Not used.	Not used.

Register Programming Technique

The ASCOR module registers listed in

Table 9-2 are accessed under VXI A24/ A32 Address Mode as 16-bit words or 32-bit words. Since all 16 bits or 32 bits are programmed with a single write operation, care must be taken to preserve the state of bits that effect other functions. In order to avoid changing any other bits in a register use the following procedure:

1. Read the register first into memory.
1. Write only to the bit(s) in memory that you intend to change.
2. Write the new value back to the register.

Programming Examples

Example 1. Obtains the A24 Base Address using National Instruments NI-VXI GetDevInfo.

Procedure obtains the A24 Base Address using its base. The Logical Address is 5.

```
/* C code segment for obtaining the device's A24 Base Address */

int16    ret;
uint16    la        = 5;        /* Logical Address */
uint16    field     = 12;       /* Base of A24 address space */
uint32    baseA24;

/* Get the A24 Base Address */
ret = GetDevInfo (la, field, &baseA24);

/* Check for function error /
if (ret < 0)
    /* Error occurred during GetDevInfo. */;
```

Example 2. Obtains the A32 Base Address using National Instruments NI-VXI GetDevInfo.

Procedure obtains the A32 Base Address using its base. The Logical Address is 5.

```
/* C code segment for obtaining the device's A32 Base Address */

int16    ret;
uint16    la        = 5;        /* Logical Address */
uint16    field     = 12;       /* Base of A32 address space */
uint32    baseA32;

/* Get the A32 Base Address */
ret = GetDevInfo (la, field, &baseA32);

/* Check for function error */
if (ret < 0)
    /* Error occurred during GetDevInfo.*/;
```

Example 3. Writes to the first module register using National Instruments NI-VXI calls, A24 Address Mode, and 16-bit data.

Procedure writes the value 1000h to the first module register. The A24 Base Address is 200000h.

```

/* C code segment for writing the value 0x1000h to the first module */
/* Register, assuming an A24 Base Address of 200000h */

int16    ret;
uint16    accessparms    =2; /* A24, Nonprivileged data access, */
                                /* Motorola Byte Order */

uint32    address;
uint16    width          =2; /* width = word (16 bits) */
uint32    value32;

address = 0x208000;          /* A24 Base Address + first module */
                                /* Register offset */
value32 = 0x1000;           /* Value to write to the first module */
                                /* Register */

/* Write to the First module register. */
ret = VXIout (accessparms, address, width, value32);

/* Check for write error. */
if (ret<0)
    /* Error occurred during write. */;

```

Example 4. Writes to the first module register using VXIplug&play VISA calls, A24 Address Mode, and 16-bit data.

Procedure writes the value 2000h to the first module register. The variable, "vi" references the Logical Address.

```
/* C code segment for writing the value 0x2000 to the first module */
/* Register */

ViStatus      as3xxx_status;
ViSession     vi;                                /* vi from previous call to */
                                                    /* as3xxx_init */
ViUInt16      space=VI_A24_SPACE; /* A24 Address Space */
ViBusAddress   offset=0x8000;    /* first module register offset. */
ViUInt16      value16;

value16 = 0x2000;                                /* Value to write to the first */
                                                    /* module register */

/* Write to the first module register. */
as3xxx_status = ViOut16 (vi, space, offset, value16);

/* Check for write error. */
if (as3xxx_status < VI_SUCCESS)
    /* Error occurred during write. */;
```

Example 5. Writes to the first module register using National Instruments NI-VXI calls, A32 Address Mode, and 32-bit data.

Procedure writes the value 10000h to the first module register. The A32 Base Address is 20000000h.

```

/* C code segment for writing the value 0x10000000 to the first */
/* module register, assuming an A32 Base Address of 20000000h */

int16    ret;
uint16    accessparms    =3; /* A32, Nonprivileged data access, */
                                /* Motorola Byte Order */

uint32    address;
uint16    width          =4; /* width = long word (32 bits) */
uint32    value32;

address = 0x20008000;          /* A32 Base Address + first module */
                                /* register offset */
value32 = 0x10000;             /* Value to write to the first module */
                                /* register */

/* Write to the First module register. */
ret = VXIout (accessparms, address, width, value32);

/* Check for write error. */
if (ret<0)
    /* Error occurred during write. */;
```

Example 6. Writes to the first module register using VXIplug&play VISA calls, A32 Address Mode, and 32-bit data.

Procedure writes a value to all bits of the first module register, assuming that A32 Address Space is configured. The variable, "vi" references the Logical Address.

```
/* C code segment for writing the value 0x10000000 to the first */
/* module register */

ViStatus      as3xxx_status;
ViSession     vi;                /* vi from previous call to */
                                   /* as3xxx_init */
ViUInt16      space=VI_A32_SPACE; /* A32 Address Space */
ViBusAddress   offset=0x8000;     /* first module register offset. */
ViUInt32      value32;

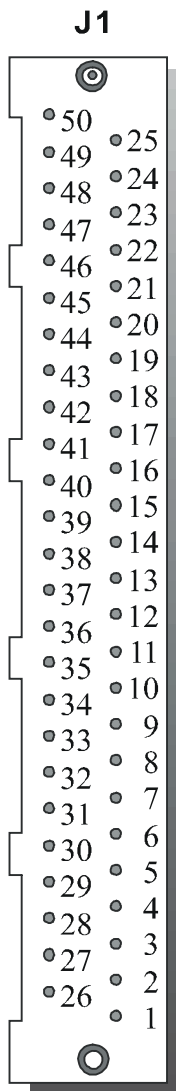
Value32 = 0x10000000;            /* Value to write to the first module */
                                   /* register */

/* Write to the first module register. */
as3xxx_status = ViOut32 (vi, space, offset, value32);

/* Check for write error. */
if (as3xxx_status < VI_SUCCESS)
    /* Error occurred during write. */;
```

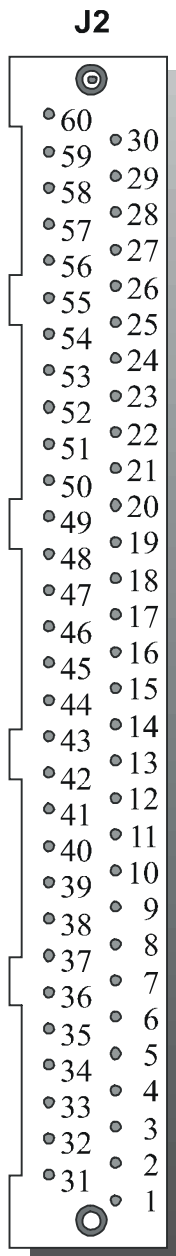
Chapter 10 Front Panel Connector

10.1 J1 Pin Signals



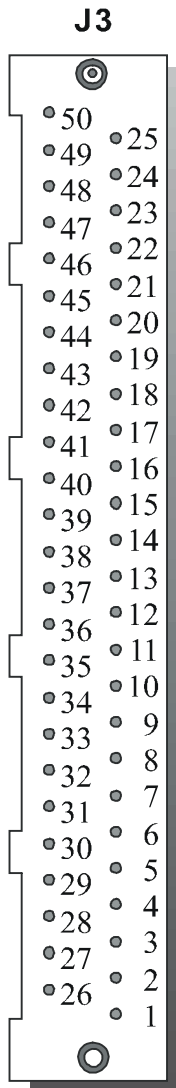
Pin	Function
1	NC
2	PIN 16 SHIELD
3	PIN 16 LO
4	PIN 16 HI
5	PIN 14 SHIELD
6	PIN 14 LO
7	PIN 14 HI
8	PIN 12 SHIELD
9	PIN 12 LO
10	PIN 12 HI
11	PIN 10 SHIELD
12	PIN 10 LO
13	PIN 10 HI
14	PIN 8 SHIELD
15	PIN 8 LO
16	PIN 8 HI
17	PIN 6 SHIELD
18	PIN 6 LO
19	PIN 6 HI
20	PIN 4 SHIELD
21	PIN 4 LO
22	PIN 4 HI
23	PIN 2 SHIELD
24	PIN 2 LO
25	PIN 2 HI
26	NC
27	PIN 15 SHIELD
28	PIN 15 LO
29	PIN 15 HI
30	PIN 13 SHIELD
31	PIN 13 LO
32	PIN 13 HI
33	PIN 11 SHIELD
34	PIN 11 LO
35	PIN 11 HI
36	PIN 9 SHIELD
37	PIN 9 LO
38	PIN 9 HI
39	PIN 7 SHIELD
40	PIN 7 LO
41	PIN 7 HI
42	PIN 5 SHIELD
43	PIN 5 LO
44	PIN 5 HI
45	PIN 3 SHIELD
46	PIN 3 LO
47	PIN 3 HI
48	PIN 1 SHIELD
49	PIN 1 LO
50	PIN 1 HI

10.2 Front Panel Connector J2 Pin Signals



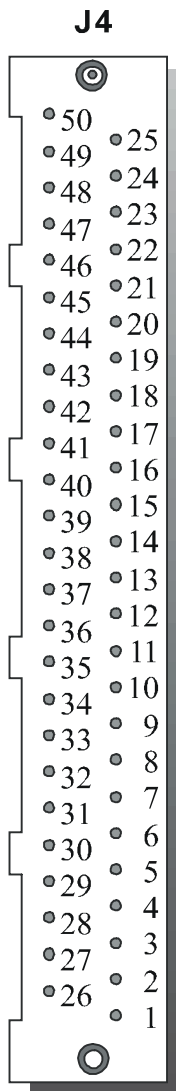
Pin	Function
1	CHAN D BUS - SHIELD
2	CHAN D HI
3	CHAN D LO
4	CHAN C BUS - SHIELD
5	CHAN C HI
6	CHAN C LO
7	PIN 32 SHIELD
8	PIN 32 LO
9	PIN 32 HI
10	PIN 30 SHIELD
11	PIN 30 LO
12	PIN 30 HI
13	PIN 28 SHIELD
14	PIN 28 LO
15	PIN 28 HI
16	PIN 26 SHIELD
17	PIN 26 LO
18	PIN 26 HI
19	PIN 24 SHIELD
20	PIN 24 LO
21	PIN 24 HI
22	PIN 22 SHIELD
23	PIN 22 LO
24	PIN 22 HI
25	PIN 20 SHIELD
26	PIN 20 LO
27	PIN 20 HI
28	PIN 18 SHIELD
29	PIN 18 LO
30	PIN 18 HI
31	CHAN B BUS - SHIELD
32	CHAN B HI
33	CHAN B LO
34	CHAN A BUS - SHIELD
35	CHAN A HI
36	CHAN A LO
37	PIN 31 SHIELD
38	PIN 31 LO
39	PIN 31 HI
40	PIN 29 SHIELD
41	PIN 29 LO
42	PIN 29 HI
43	PIN 27 SHIELD
44	PIN 27 LO
45	PIN 27 HI
46	PIN 25 SHIELD
47	PIN 25 LO
48	PIN 25 HI
49	PIN 23 SHIELD
50	PIN 23 LO
51	PIN 23 HI
52	PIN 21 SHIELD
53	PIN 21 LO
54	PIN 21 HI
55	PIN 19 SHIELD
56	PIN 19 LO
57	PIN 19 HI
58	PIN 17 SHIELD
59	PIN 17 LO
60	PIN 17 HI

10.3 Table 10-1. Front Panel Connector J3 Pin Signals



Pin	Function
1	NC
2	PIN 48 SHIELD
3	PIN 48 LO
4	PIN 48 HI
5	PIN 46 SHIELD
6	PIN 46 LO
7	PIN 46 HI
8	PIN 44 SHIELD
9	PIN 44 LO
10	PIN 44 HI
11	PIN 42 SHIELD
12	PIN 42 LO
13	PIN 42 HI
14	PIN 40 SHIELD
15	PIN 40 LO
16	PIN 40 HI
17	PIN 38 SHIELD
18	PIN 38 LO
19	PIN 38 HI
20	PIN 36 SHIELD
21	PIN 36 LO
22	PIN 36 HI
23	PIN 34 SHIELD
24	PIN 34 LO
25	PIN 34 HI
26	NC
27	PIN 47 SHIELD
28	PIN 47 LO
29	PIN 47 HI
30	PIN 45 SHIELD
31	PIN 45 LO
32	PIN 45 HI
33	PIN 43 SHIELD
34	PIN 43 LO
35	PIN 43 HI
36	PIN 41 SHIELD
37	PIN 41 LO
38	PIN 41 HI
39	PIN 39 SHIELD
40	PIN 39 LO
41	PIN 39 HI
42	PIN 37 SHIELD
43	PIN 37 LO
44	PIN 37 HI
45	PIN 35 SHIELD
46	PIN 35 LO
47	PIN 35 HI
48	PIN 33 SHIELD
49	PIN 33 LO
50	PIN 33 HI

10.4 Table 10-1. Front Panel Connector J4 Pin Signals



Pin	Function
1	NC
2	PIN 64 SHIELD
3	PIN 64 LO
4	PIN 64 HI
5	PIN 62 SHIELD
6	PIN 62 LO
7	PIN 62 HI
8	PIN 60 SHIELD
9	PIN 60 LO
10	PIN 60 HI
11	PIN 58 SHIELD
12	PIN 58 LO
13	PIN 58 HI
14	PIN 56 SHIELD
15	PIN 56 LO
16	PIN 56 HI
17	PIN 54 SHIELD
18	PIN 54 LO
19	PIN 54 HI
20	PIN 52 SHIELD
21	PIN 52 LO
22	PIN 52 HI
23	PIN 50 SHIELD
24	PIN 50 LO
25	PIN 50 HI
26	NC
27	PIN 63 SHIELD
28	PIN 63 LO
29	PIN 63 HI
30	PIN 61 SHIELD
31	PIN 61 LO
32	PIN 61 HI
33	PIN 58 SHIELD
34	PIN 58 LO
35	PIN 58 HI
36	PIN 57 SHIELD
37	PIN 57 LO
38	PIN 57 HI
39	PIN 55 SHIELD
40	PIN 55 LO
41	PIN 55 HI
42	PIN 53 SHIELD
43	PIN 53 LO
44	PIN 53 HI
45	PIN 51 SHIELD
46	PIN 51 LO
47	PIN 51 HI
48	PIN 49 SHIELD
49	PIN 49 LO
50	PIN 49 HI